

S/N 09/834751

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Sergey A. Velichko et al. Examiner: Craig Steven Miller  
Serial No.: 09/834751 Group Art Unit: 2812  
Filed: April 13, 2001' Docket: 303.750US1  
Title: CONCURRENT CONTROL OF SEMICONDUCTOR PARAMETRIC TESTING

**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(c)(2), Applicants have included the fee of \$180.00 as set forth in 37 C.F.R. §1.17(p). Please charge any additional fees or credit any overpayment to Deposit Account No. 19-0743.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

SERGEY A. VELICHKO ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLOTH, P.A.  
P.O. Box 2938  
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(612) 349-9581

Date

Jan 28 '04

By

[Signature]

John M. Dahl

Reg. No. 44,639

**CERTIFICATE UNDER 37 CFR 1.8:** The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 28th day of January, 2004.

Name

Amy Moravsky

Signature

[Signature]

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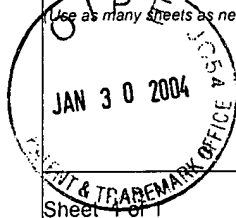
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Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)



Complete if Known

Application Number	09/834751
Filing Date	April 13, 2001
First Named Inventor	Velichko, Sergey
Group Art Unit	2812
Examiner Name	Miller, Craig

Attorney Docket No: 303.750US1

**US PATENT DOCUMENTS**

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US20030028343	02/06/2003	Velichko, Sergey A., et al.	702	122	04/25/2002
	US20030212523	11/13/2003	Dorough, Michael J., et al.	702	119	04/25/2002
	US-5,241,266	08/31/1993	Ahmad, A. , et al.	714	733	04/10/1992
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	US-5,787,190	07/28/1998	Peng, Y. , et al.	382	145	06/27/1997
	US-5,869,974 ,	02/09/1999	Akram, Salman , et al.	324	754	04/01/1996
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	US-6,383,825	05/07/2002	Farnworth, Warren M., et al.	438	14	07/10/2001
	US-6,445,199	09/03/2002	Satya, A. V., et al.	324	753	08/25/2000
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	US-6,507,800	01/14/2003	Sheu, S.	702	117	03/13/2000
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	US-6,618,682	09/09/2003	Bulaga, R. J., et al.	604	27	04/20/2001
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	US-6,629,282	09/30/2003	Sugamori, S. , et al.	714	734	11/05/1999
	US-6,639,417	10/28/2003	Takao, T.	324	765	06/26/2001

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**OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS**

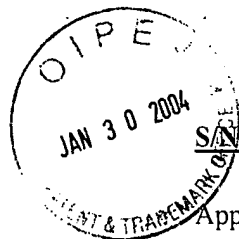
Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		BLUNN, R G., "Concurrent fault tolerant control of semiconductor measurement and testing", 2001 IEEE International Semiconductor Manufacturing Symposium, (October 8-10, 2001),455-458	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup> Applicant's unique citation designation number (optional) <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached



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COMMUNICATION CONCERNING RELATED APPLICATION(S)

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
10/131934	April 25, 2002	303.771US1	INTELLIGENT MEASUREMENT MODULAR SEMICONDUCTOR PARAMETRIC TEST SYSTEM
10/133685	April 25, 2002	303.821US1	DYNAMICALLY ADAPTABLE SEMICONDUCTOR PARAMETRIC TESTING
10/417640	April 17, 2003	303.855US1	DYNAMIC CREATION AND MODIFICATION OF WAFER TEST MAPS DURING WAFER TESTING

Respectfully submitted,

SERGEY A. VELICHKO ET AL.

By Applicants' Representatives,

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Date

Jan 28 04

By

John M. Dahl

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Reg. No. 44,639

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Name

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Signature

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